

A cross-sectional view of a semiconductor device. A central gate structure (1) is formed on a substrate (3). The gate structure includes a gate dielectric (2) and a gate electrode (1). A central channel region (8) is located beneath the gate electrode. On either side of the central gate structure, there are side regions (3a, 3b, 3c, 3d). A central contact region (7) is located beneath the gate structure. A central contact pad (6) is located on the side of the central gate structure. A central contact pad (4) is located on the side of the side region (3a). A central contact pad (5) is located on the side of the side region (3b). A central contact pad (3d) is located on the side of the side region (3c). A central contact pad (3) is located on the side of the side region (3a).

A detailed cross-sectional diagram of a semiconductor device. At the center is a vertical core structure (2) consisting of multiple stacked rectangular blocks. This core is surrounded by a thick substrate (8). On the left and right sides, there are complex layered structures (7 and 8 respectively) that appear to be part of a bonding or encapsulation process. These structures include various thin films, solder bumps (7b, 8a), and underlayers (7e, 8e). Labels like R1 and R2 point to specific regions within these side structures. A dashed horizontal line indicates a plane of symmetry. Arrows labeled B and T indicate specific directions or forces. Various other labels (1, 2c, 2d, 3a, 3b, 3c, 3d, 3e, 4, 5, 6, 7c, 7c1, 8c, 8d, 8d1, 9) identify different components and interfaces within the assembly.

FIG. 3

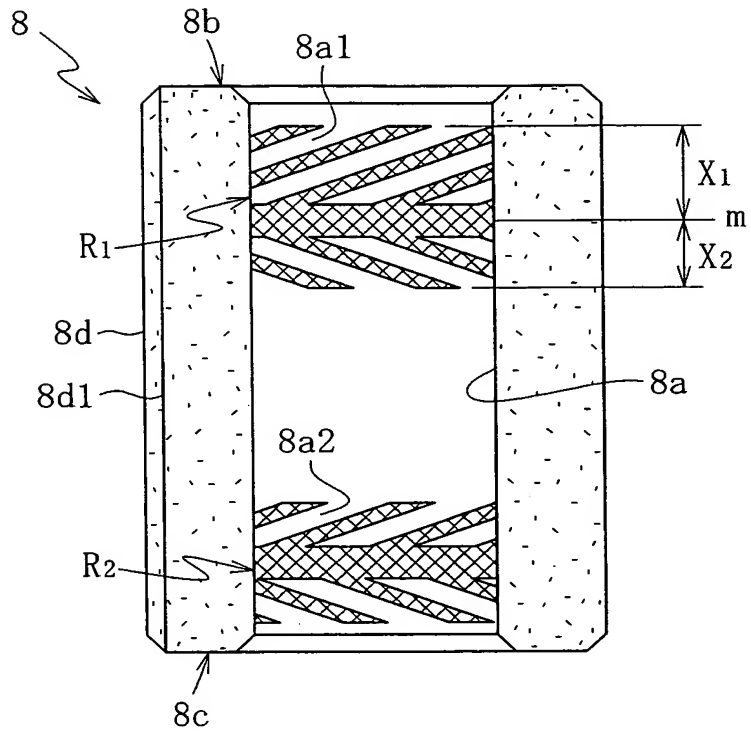


FIG. 4

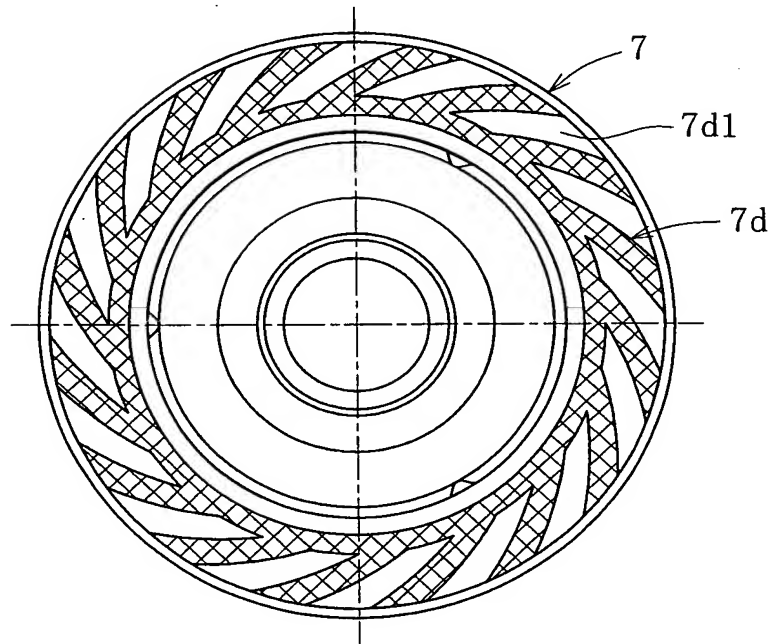


FIG. 5

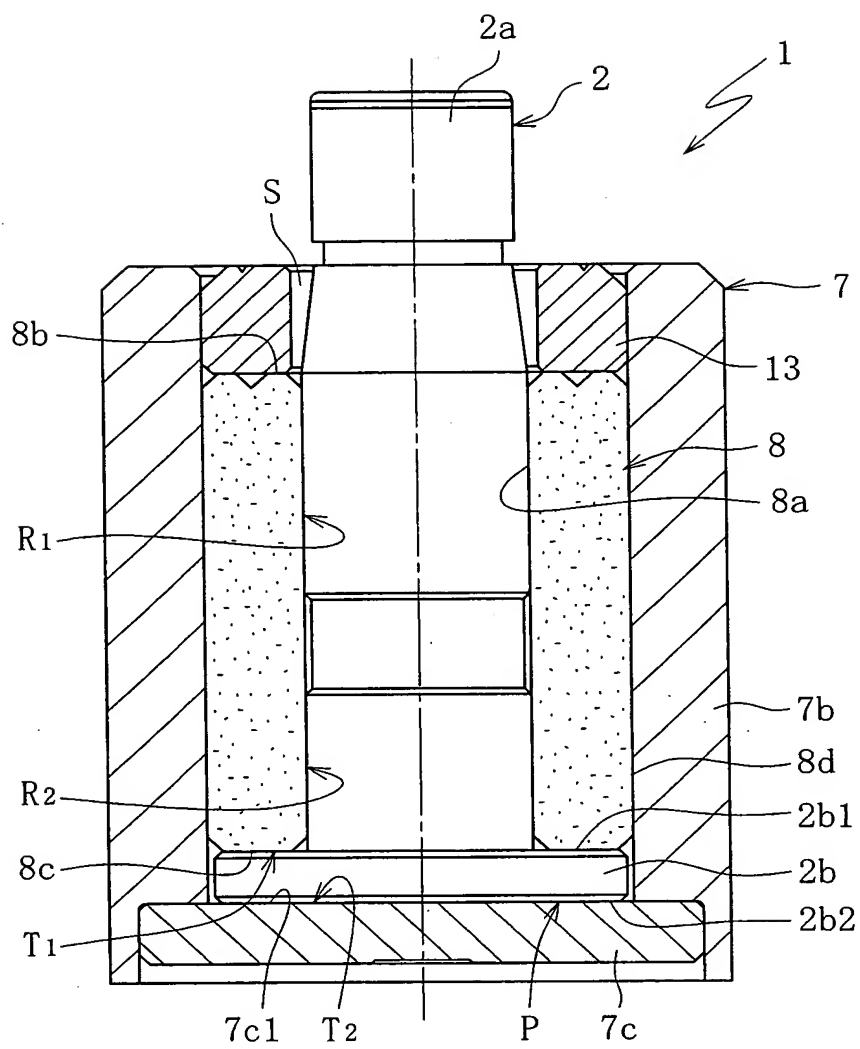


FIG. 6



FIG. 7



FIG. 8a

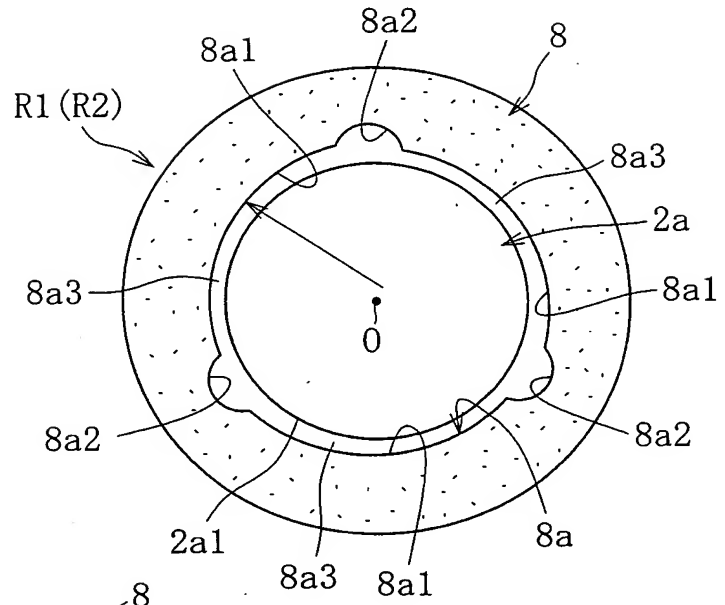


FIG. 8b

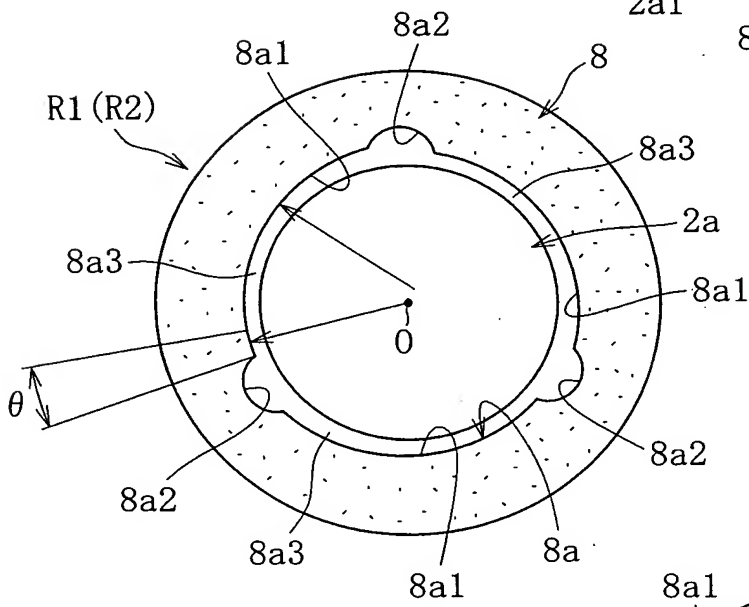
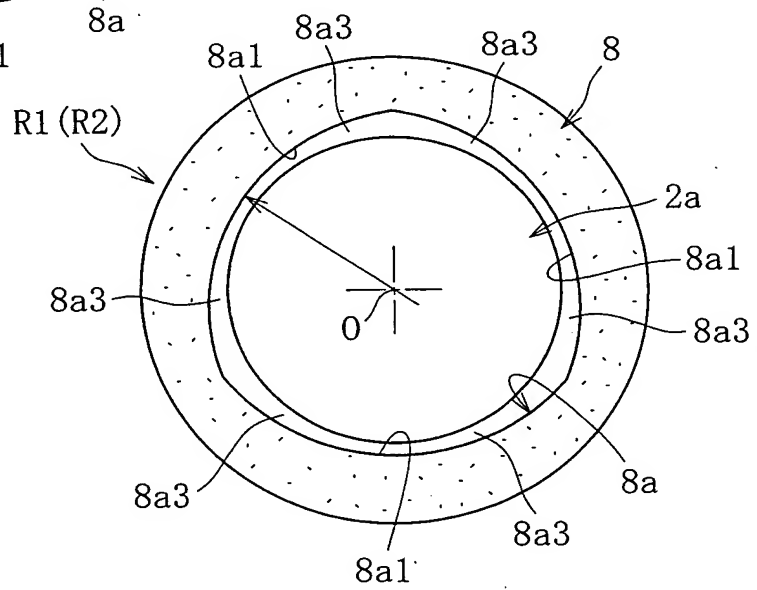


FIG. 8c



[illegible]

FIG. 11a

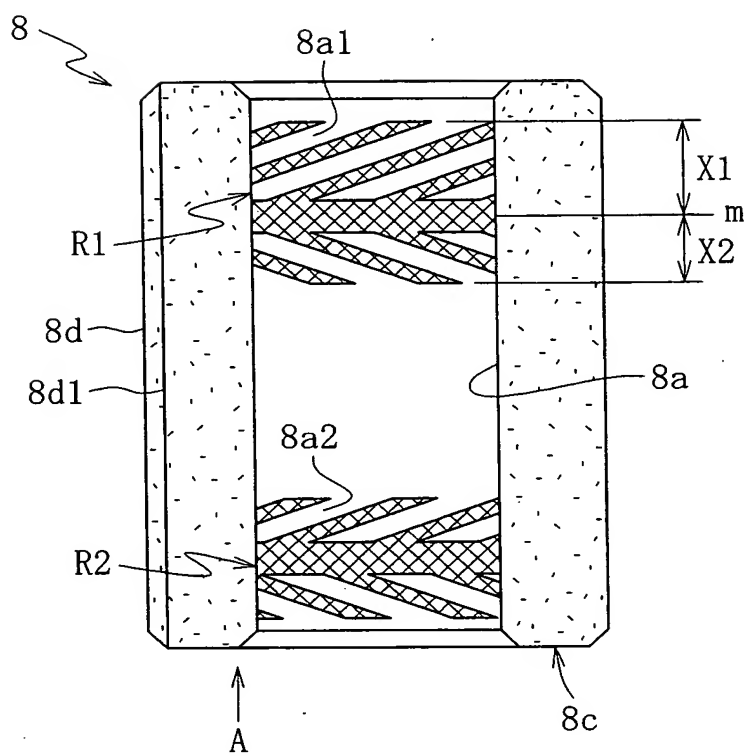


FIG. 11b

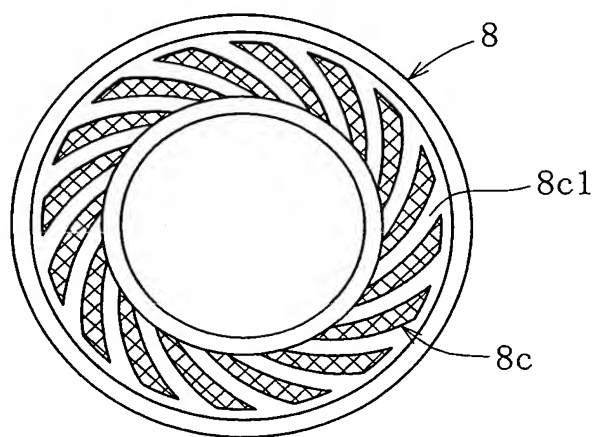


FIG. 12

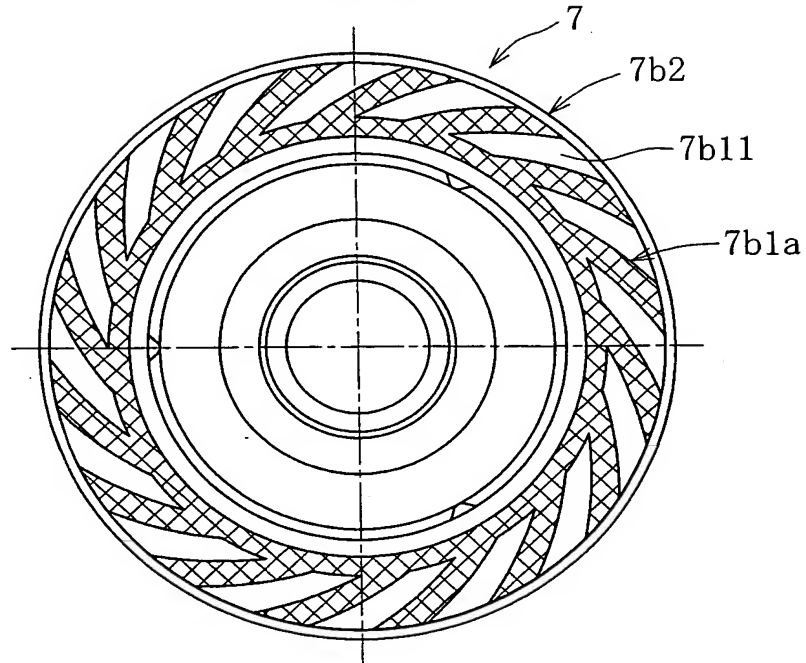


FIG. 13

